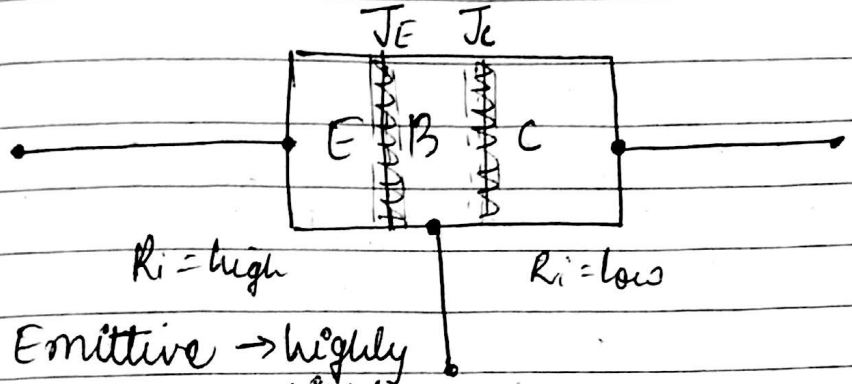
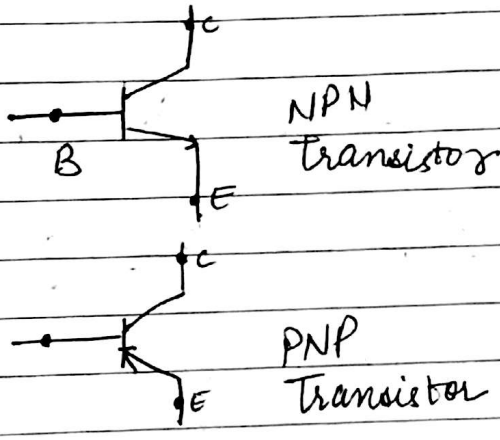
Bipolar junction Transistor (BJT)



E = Emittive → highly
B = Base → lightly
C = Collector → medium

Symbol



- Bipolar
  - ↳ current flows due to two types of charge carriers i.e electrons & holes

Trans carriers flow from high Resistance region to low resistance → Transistor
& vice versa

* Emitter: Source of charge carriers (medium area)
* Base:- of Base is heavily doped as Emitter base & Base are of opposite nature (P-N) or (N-P)
  to Base is lightly doped to reduce combination of holes & e⊖ → Base size is short (small)
* → Time taken by charge carriers to cross base called as Transit time
  - Time may less so area is small

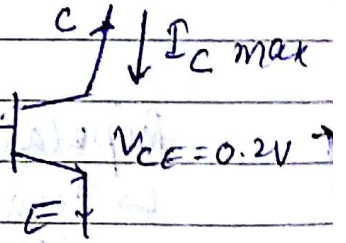
* Collection :- Kept large and medium doped as charge carriers are already present & more charriers will come as more charge carriers are present in collector So due to collision, Energy generated which dissipate power to move in different direction so if the collector region will be large ~~big~~ then the Area will be more which consequently helps in less collision

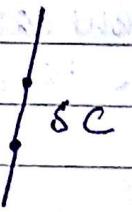
* for Amplifying we need the configuration of n-p-n & p-n-p.

Different Biasing Transistor

① J_E J_C

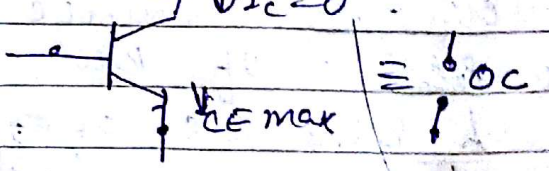
FB FB → Saturation Region





② J_E J_C

R_B R_B Cutoff Region



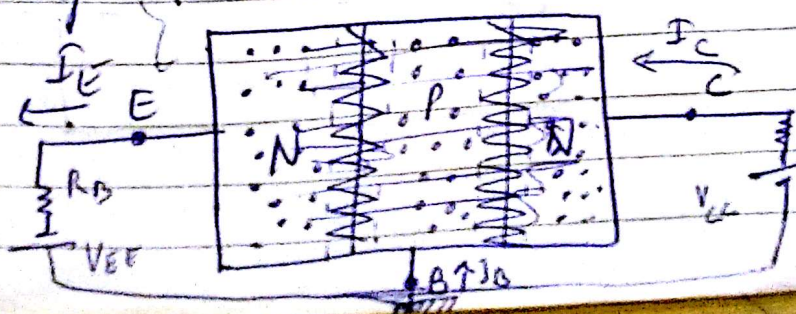
③ J_E J_C forward → Active Region → Transistor behaves as Amplifier
FB RB

④ J_E J_C
RB FB → Reverse Active Region → Gain is negligible so trans. cannot be used as Amplifier

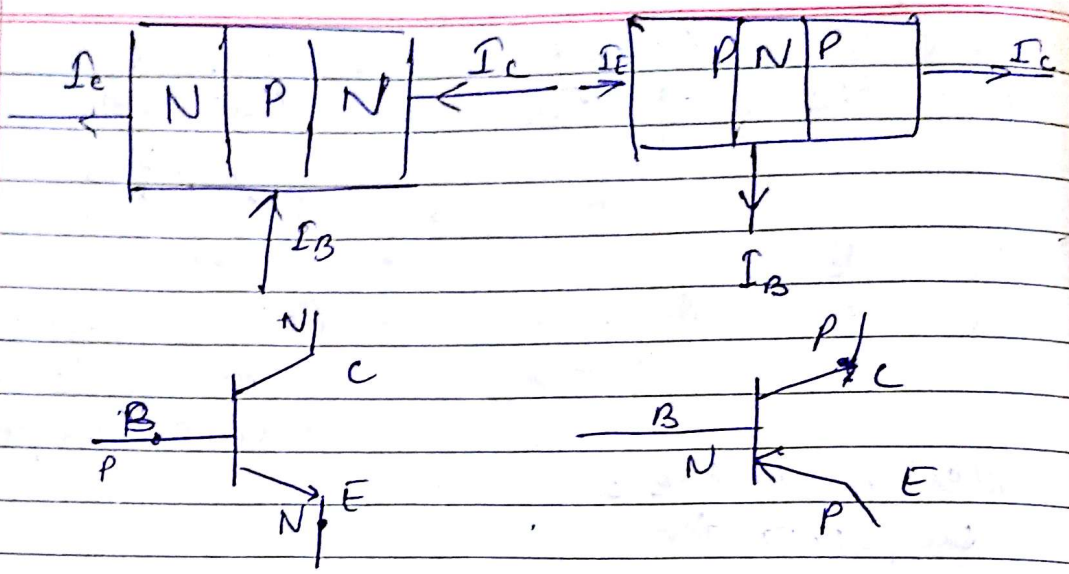
- External voltage supply which is supplied to device Biasing

Introduction of BJT

* BJT stands for Bipolar junction Transistor)
* It is a Bipolar device i.e. current is carried by both e⊖ & holes so it has both majority carriers & minority carriers. It is a three layer 2 junction device first junction is formed b/w Ammeter & Base second junction is formed b/w base & collector
* Ammeter is highly doped to inject its majority carriers into base & is provided with medium area
* Base is lightly doped to reduce the recombination & is provided with smallest Area to reduce the transit time It is the time taken by charge carriers in moving from Ammeter to collector
* Collector is moderately doped & it is provided with largest Area to withstand heat dissipation.

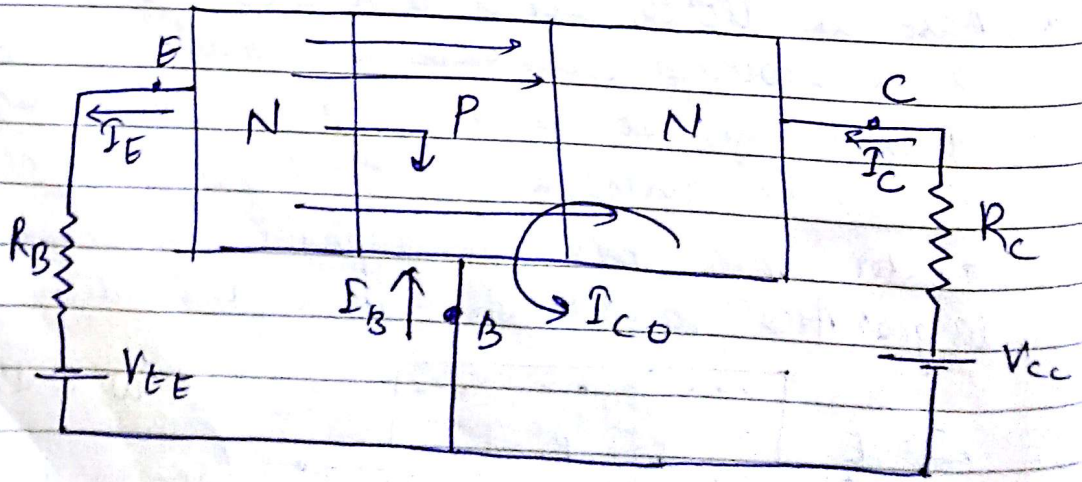


W = width of depletion layer
$W \propto \frac{1}{\text{Doping Concentration}}$



$$I_E = I_B + I_C$$

- In N-P-N Transistor current is dominated by $e^{\ominus}$, In P-N-P Transistor current is dominated by holes
- NPN & PNP transistor complementary transistor because direction of current majority carriers & voltages are opposite in both cases



Diffusion Current :- $I_E I_B, I_C$

Drift Current or leakage Current :- I_{CO}
Reverse saturation Current

There are two types of current which flows in Transistor

1. Diffusion Current
When charge carriers move from highly-doped region to low doped Region. This current generated is Diffusion Current

OR

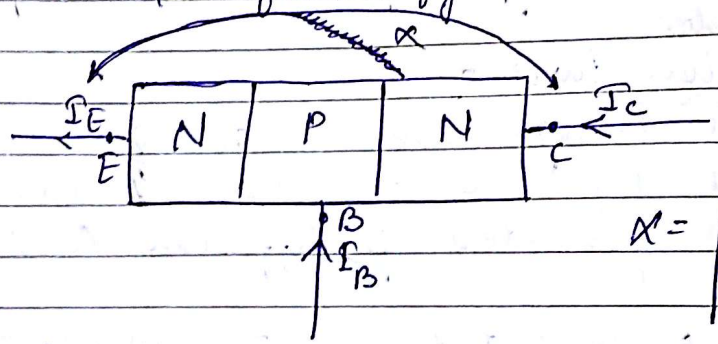
Current generated due to majority charge carriers { Emitter, Base & Collector is due to movement majority carriers }

2. Drift Current - I_{CO} is due to movement of minority charge carriers so it is drift current

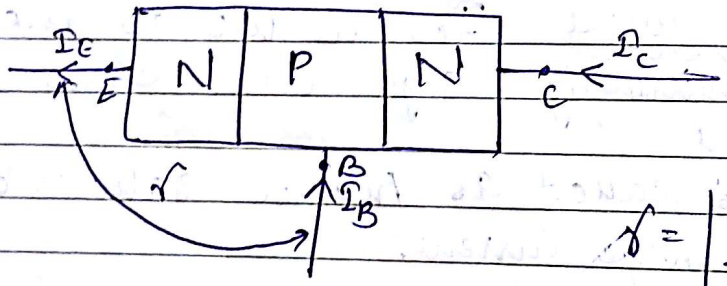
I_{CO} is called as Reverse saturation Current or Leakage Current.

Gains of Transistor

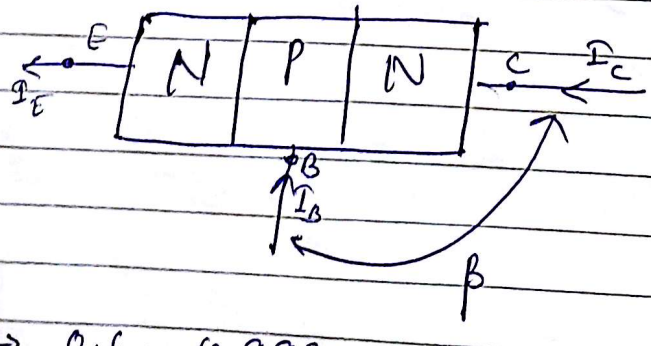
1) Alpha (α) → Gains of CB Config
2) Beta (β) → gain of CE Config
3) Gamma (γ) → Gain of CC Config



$$\alpha = \left| \frac{I_C}{I_E} \right|$$



$$\gamma = \left| \frac{I_E}{I_B} \right|$$



$$\beta = \left| \frac{I_C}{I_B} \right|$$

$\alpha \rightarrow 0.6 - 0.999$

typical value of $\alpha \rightarrow 0.98$

Gains

A_I ↘ A_V

$A_P = A_I A_V$

$\beta \Rightarrow$ 30-300

typical value $\rightarrow$ 49

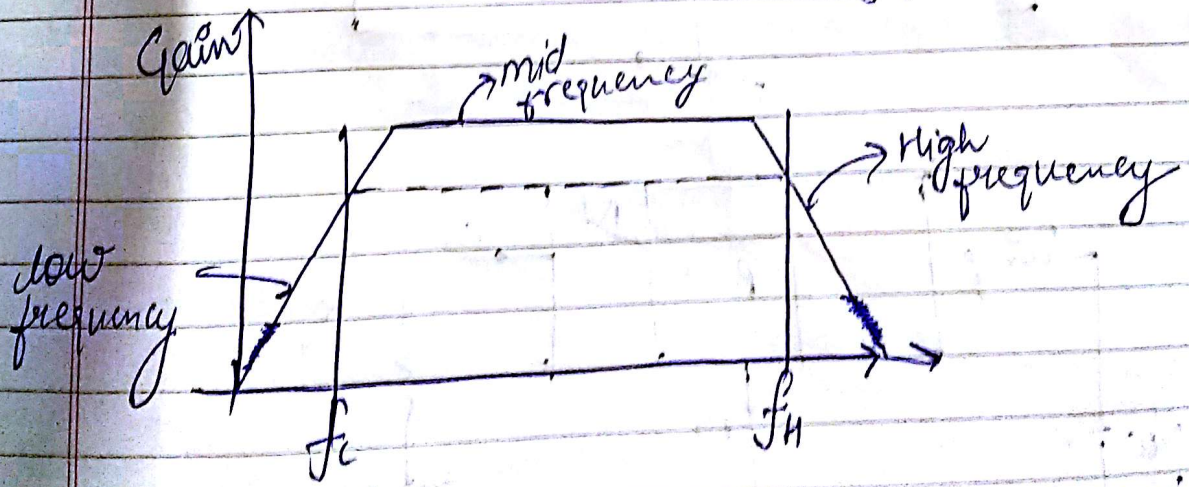
$\gamma \Rightarrow \beta + 1$ $\qquad$ $\gamma = \beta + 1$

- α is called as current gain of common Base transistor it is slightly less than 1. α ranges from 0.6 to 0.999 typical value of α is 0.98. Maximum value of α is 1 (only in ideal transistor)
- β is called as current gain of common emitter configuration β ranges from 30 to 300. Its typical value is 49. β is very sensitive to temperature in germanium β doubles for every 60°C & in silicon β doubles for every 75°C.

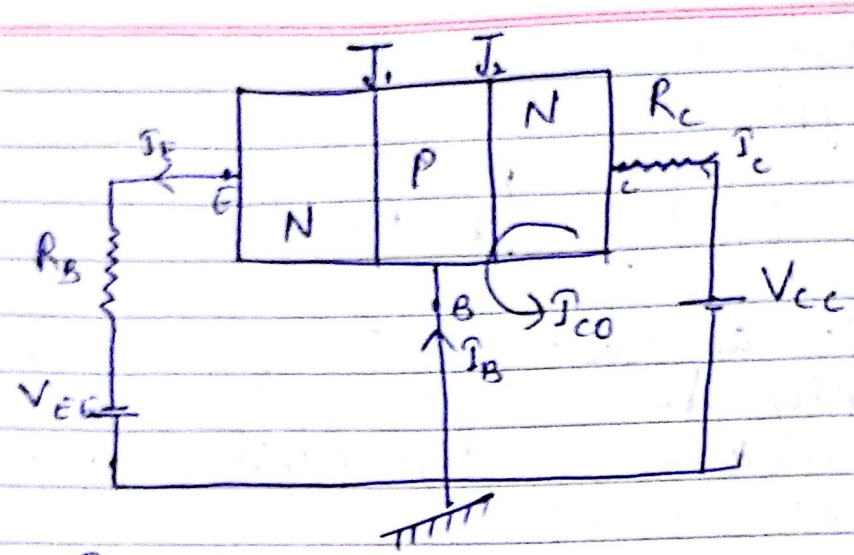
β

β_{DC} or h_{FE} $\qquad$ β_{ac} or h_{fe}

$\beta_{DC} = \left| \frac{I_C}{I_B} \right|$ $\qquad$ $\beta_{ac} = \left| \frac{\partial I_C}{\partial I_b} \right|$



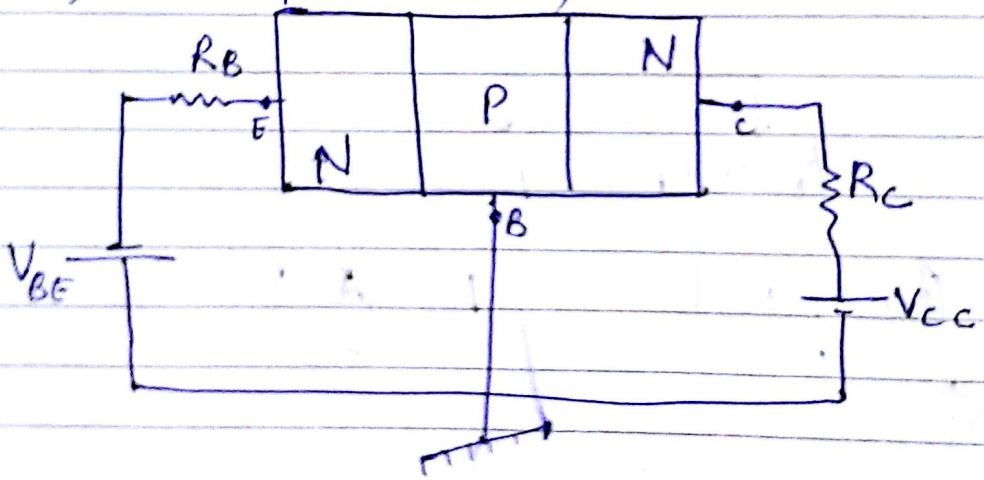
- γ is current gain of common collector transistor typical value is 50

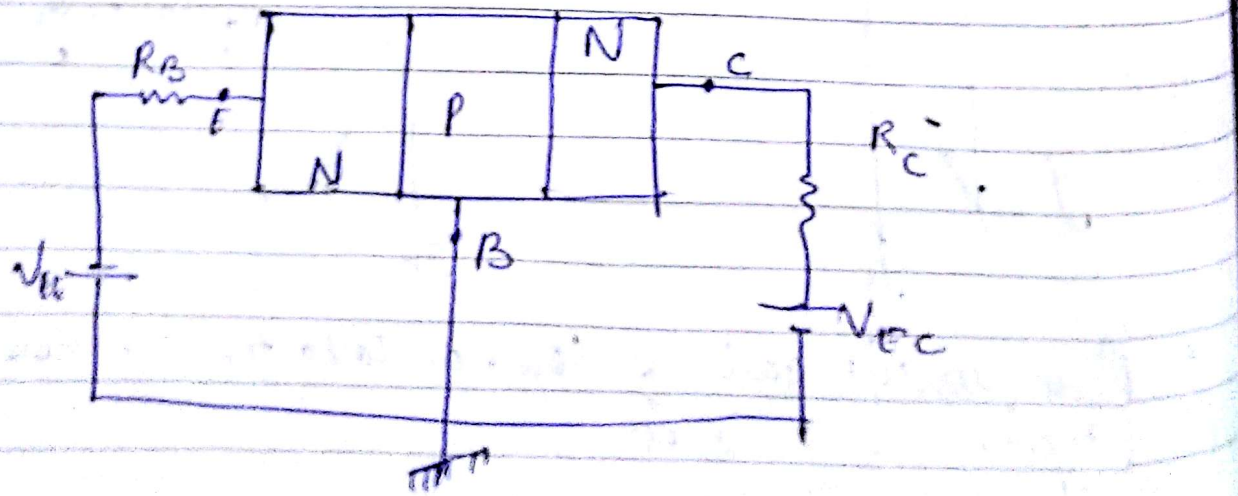


I_{CO} → Reverse saturation Current

I_{CBO} (Collector to Base Current when emitter is open circuited)

I_{CEO} (Collector to emitter Current when base is open circuited)





$I_C = \alpha I_B + I_{CO}$

for common base, $I_C = \alpha I_E + I_{CBO}$

also $I_E = I_C + I_B$

$I_C = \alpha (I_C + I_B) + I_{CBO}$

$I_C (1-\alpha) = \alpha I_B + I_{CBO}$

$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO}$

$I_C = \beta I_B + (\beta+1) I_{CBO}$

Where, $\beta = \frac{\alpha}{1-\alpha}$

1) A transistor has $\alpha = 0.98$ find its β.

$$\beta = \frac{0.98}{0.2} = 99$$

2) A transistor has $\alpha = 0.99$ find its β

$$= \frac{0.99}{0.01} = 99$$

3) A transistor has $\beta = 49$ find emitter current if $I_B = 10\mu A$

$I_C = 49 \times 10\ \mu A$

$= 49 \times 10 \times 10^{-3}\ A$

$= 0.49\ mA$

$I_E = I_B + I_C$

$I_C = \beta I_B$

$I_E = (\beta+1) I_B$

$= 50 \times 10\ \mu A$

$= 5\ mA$

$0.49 + 10$

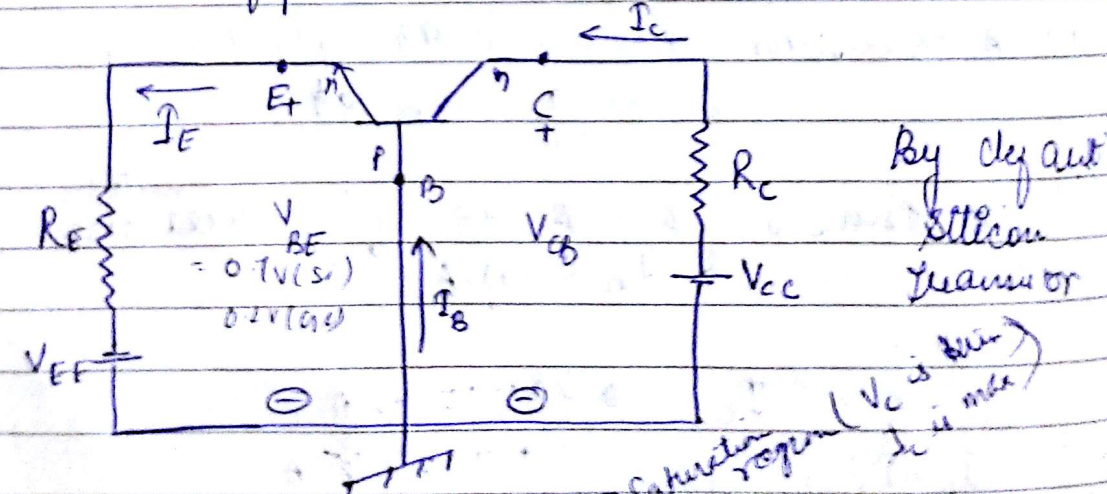
(4) Transistor has $\alpha = 0.99$; $I_B = 5\mu A$ & leakage current of 10nA find its collector current

$$I_C = 0.99 \times 5 \times 10^{-6} + 10 \times 10^{-9}$$
$$= 4.95 \times 10^{-6} + 10^{-8}$$
$$= (0.0495+1) \times 10^{-8}$$
$$= (0.0496)\, 10^{-8}$$
$$= 496\ \mu A$$

Types of configuration of BJT

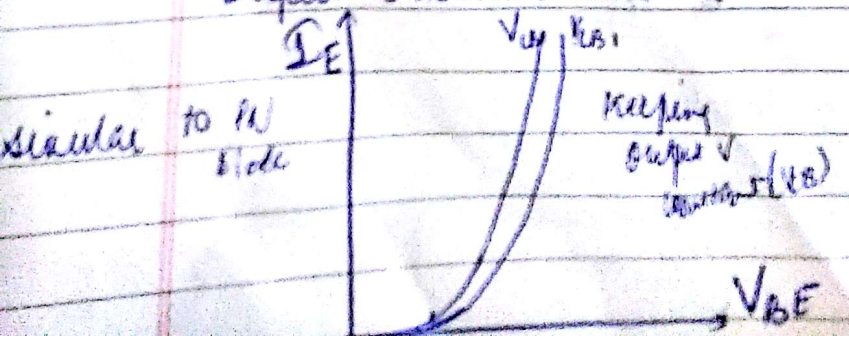
1. ★ Common Base configuration
2. Common Emitter configuration
3. Common collector configuration

Common Base Configuration

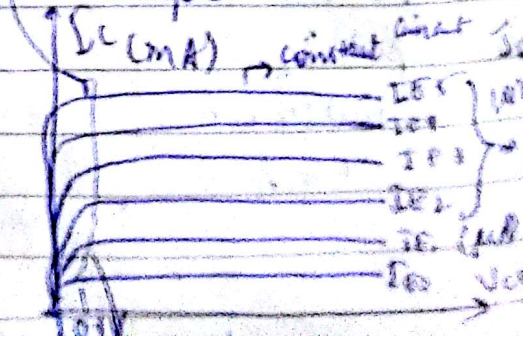


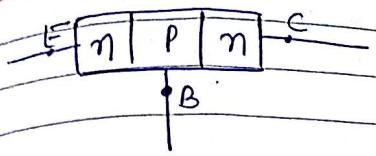
By default Silicon Transistor

Input characteristics

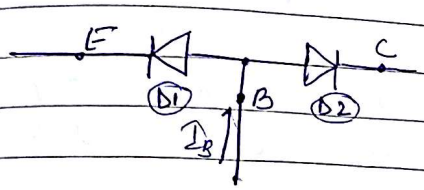


Output Characteristics





Ebers mall's Model.

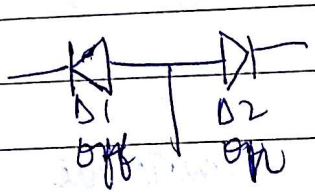


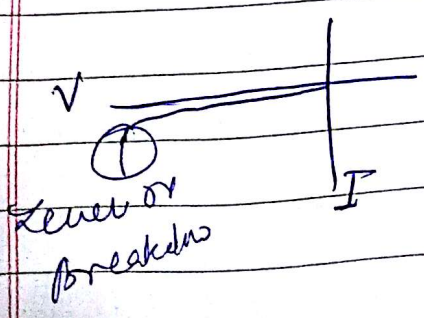
- Input characteristics of a transistor is obtained b/w input current and input voltage by keeping output voltage constant.
- Input characteristics of common base transistor is similar to the forward characteristics of diode.

Input characteristics can be explained with the help of Ebers Moll's model where two diodes D1 & D2 are connected back to back. where D1 is connected in forward bias as per the circuit given below D1 is connected in FB D2 " RB so D1 will conduct & D2 will remain off so we are getting Input characteristics of transistor similar to the forward characteristics of Diode D1

$$\text{Current Gain} = \frac{\text{Output Current}}{\text{Input Current}} = \frac{I_C}{I_E} = (\alpha = 1)$$ i.e. very less.

Output Characteristics





Output characteristics of a transistor is plotted b/w output current & output voltage by keeping input current constant.

OC curve can be divided into three region i.e saturation, Active and Cutt-off region

In saturation region IC will be maximum and V_C will be minimum. In cut-off region I_C will be minimum & V_C will be maximum

Saturation Region
$V_{CB} < 0.1V$
$I_C > 0$

Active Region $0.1 < V_{CB} < V_{CC}$
$I_E > 0$

Cut-off Region $I_E < 0$

Saturation region lies in where $V_{CB} \geq 0.1V$ and $I_C > 0$

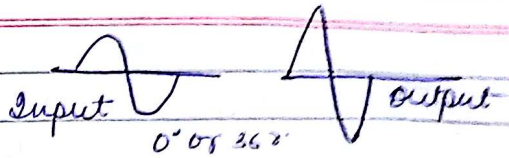
Properties of Common Base Transistor :-

1. It has lowest input resistance (less than 100 ohm).
2. It has highest output resistance (greater than 1 megaohm)
3. It has lowest current gain $A_I = \frac{I_C}{I_E} = \alpha(1)$
4. It has highest voltage gain
5. It has moderate power gain
6. (Typical value is 6B)

$A_P = A_V A_I$

moderate ← A_P ; A_V → high ; A_I → Low

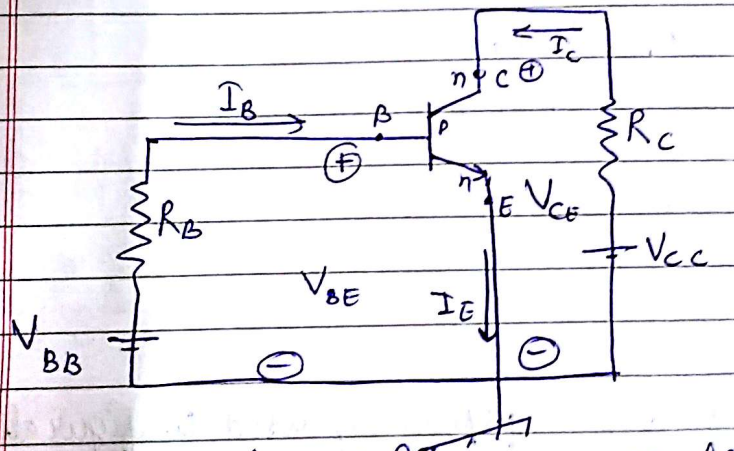
6. Phase shift is 0° or 360°



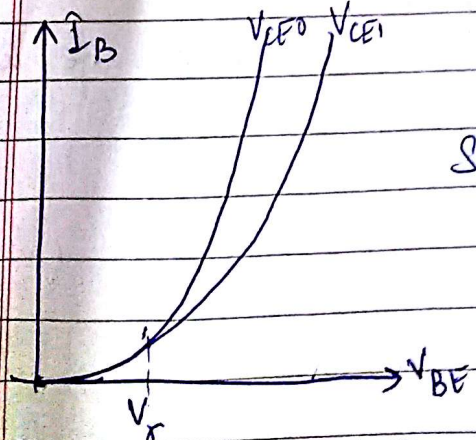
Applications :-

1. Since current is constant in output it can be used as a Constant Current Source
2. Since voltage gain is highest so it can be used as a voltage Amplifier
3. Since there is 0° or 360° phase shift so it can be used as non-inverting amplifier

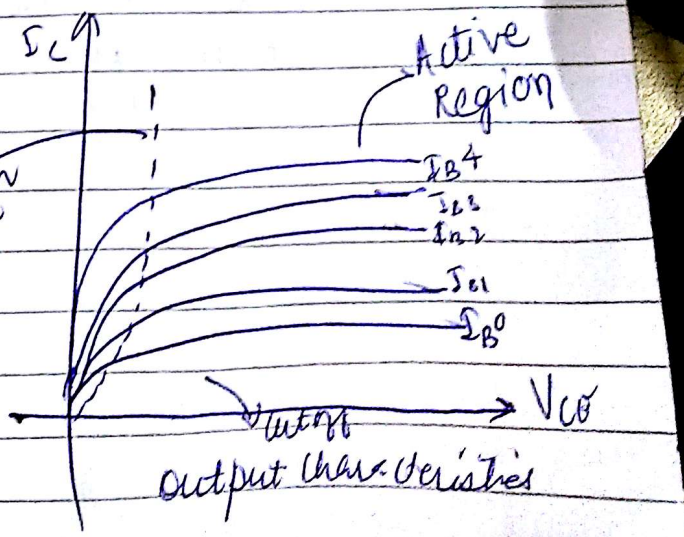
2. Common Emitter configuration



Circuit Diagram of CE Configuration



Input characteristics



Output characteristics

$$\text{Slope} = \frac{-1}{\text{Output Resistance}}$$

$$\text{Current gain} = \frac{I_C}{I_B} = \beta_0$$

Properties: ① It has moderate input resistance around (1KOhm)

② It has moderate output resistance (around 50K - 3M

③ It has moderate current Beath

④ " " voltage Beam

⑤ " highest power Beam

$$A_p = A_V A_I$$

↓ Highest ↓ moderate

⑥ It has phase shift of 180°

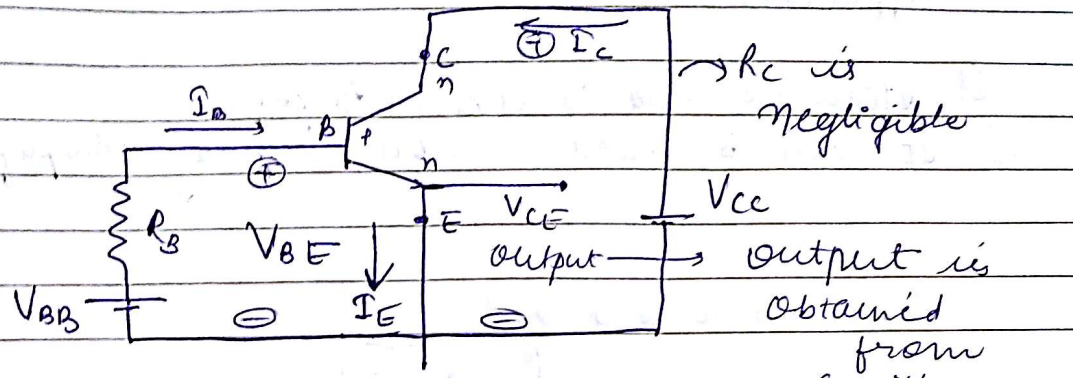
Applications

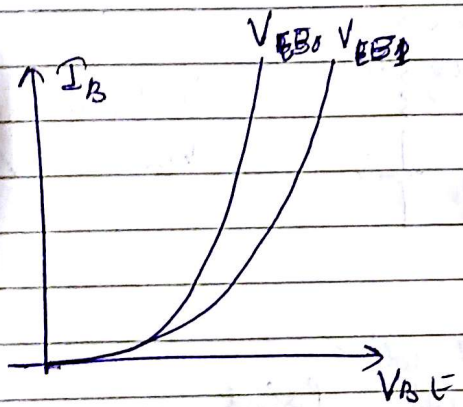
① It is most common & popularly used configuration

② since it has highest Power gain so this configuration is used Power Amplifier

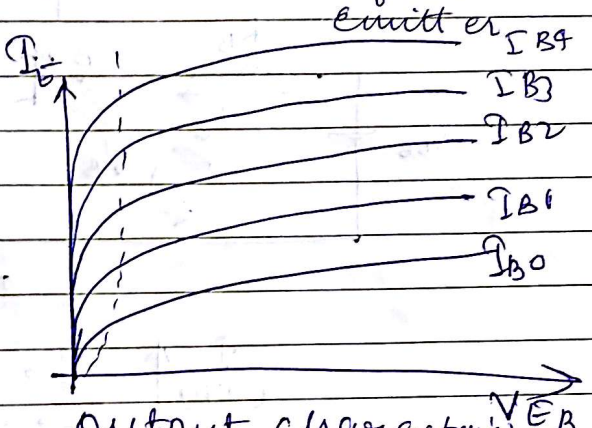
③ Since it has phase shift of 180° so it can be used as inverting Amplifier

(B) Common collector configuration

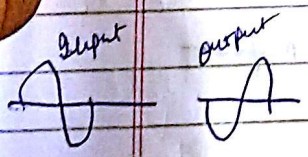




Input characteristics



Output characteristics



Current gain = $\frac{I_E}{I_B} = \gamma$

Slope = $\frac{-1}{\text{Output resistance}}$

Properties :-

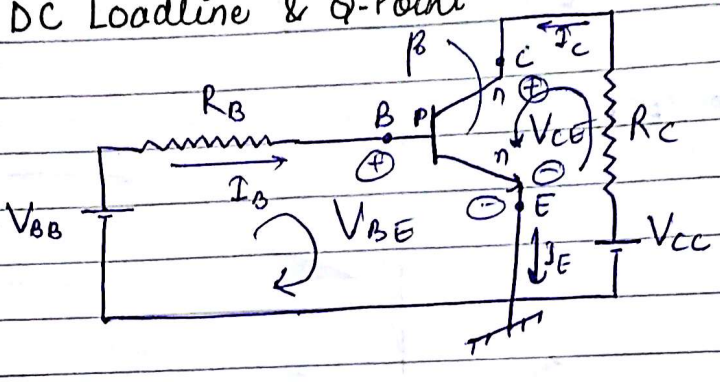
1. It has highest Input Resistance
2. It has lowest output Resistance
3. " highest current gain $A_I = \frac{I_E}{I_B} = \gamma$
4. " lowest voltage gain
5. " moderate Power gain
6. Phase shift is 0° or 360°.

Application

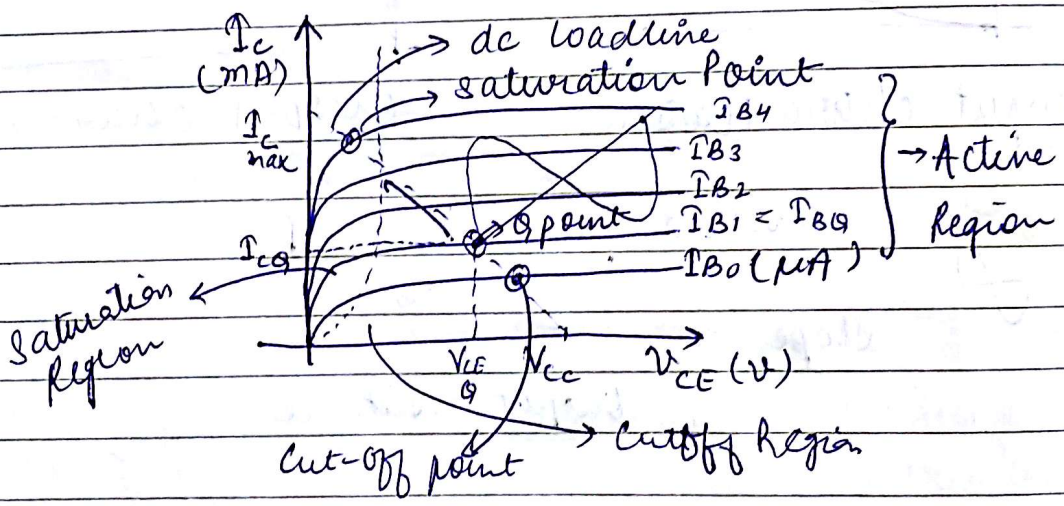
(1) It can be used as Current Amplifier
(2) It can be used as non-inverting Amplifier

...

DC Loadline & Q-Point



Si Transistor
$V_{BE} = 0.7V$



Analysis of TA

- DC Analysis (Input signal is set equal to Zero)
  To Calculate Q point, stability & operating current & voltages
- AC Analysis (DC Biasing is grounded)
  To Calculate Z_i, Z_o, A_V & A_I

Qpoint is f^n of 3 parameter (I_C, I_B, V_{CE})

Apply KVL in input loop.

$$V_{BB} - I_B R_B - V_{BE} = 0$$

$$* \boxed{I_B = \frac{V_{BB} - V_{BE}}{R_B}}$$

$$* \boxed{I_C = \beta I_B}$$

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$* \boxed{V_{CE} = V_{CC} - I_C R_C}$$

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$(I_C) = \frac{V_{CC} - (V_{CE})}{R_C}$$

for $V_{CE} = 0$

$$\boxed{I_{C_{max}} = \frac{V_{CC}}{R_C}}$$

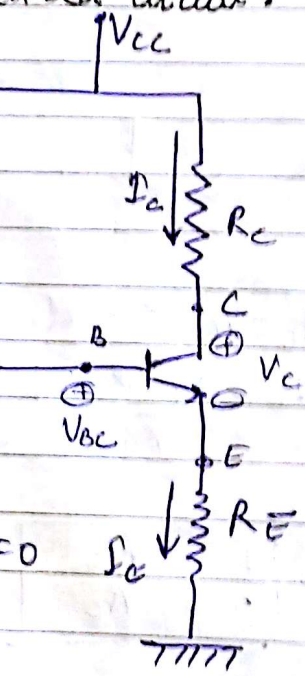
for maximum stability, should be at centre

- DC loadline is a straight line which joins I_{Cmax} & V_{CC} or saturation point & cutoff point
- DC loadline is plotted under "quescient condition" a transistor is said to be under quescient condition when zero input signal is applied
- Q point is called as quescient point or operating point It is function of I_B, I_C & V_{CE}.

- Q point is temperature sensitive as temperature increases I_C will increase & V_{CE} will increase & Q point is shift towards saturation Region so transistor will stop working as an amplifier.

similarly Q point is situated near cut-off Region then also negative half of the cycle will be clipped off & output will be distorted so to get maximum gain in amplifier with distortion less output Q point must be located at the centre of DC loadline.

2 Emitter stabilized circuit:-



Applying KVL in I/P loop

$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$

$I_E = (\beta+1) I_B$

$V_{CC} - I_B R_B - V_{BE} - (\beta+1) I_B R_E = 0$

$V_{CC} - I_B(R_B + (\beta+1) R_E) - V_{BE} = 0$

$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta+1) R_E}$

$I_C = \beta I_B$

Apply KVL in O/P loop

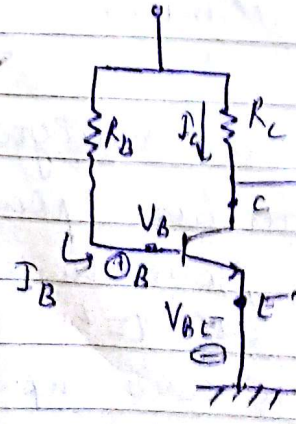
$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$

$\star [I_C \simeq I_E]$

$V_{CC} - I_C(R_C + R_E) - V_{CE} = 0$

$V_{CE} = V_{CC} - I_C(R_C + R_E)$

Fixed Bias Circuit:-



$I_C = \beta I_B$

Applying KVL in O/P loop

$V_{CC} - I_C R_C - V_{CE} = 0$

$[V_{CE} = V_{CC} - I_C R_C]$

also $V_{CE} = V_C - V_E$

$V_{BE} = V_B - V_E$

$V_{BC} = V_B - V_C$

Applying KVL in I/P loop

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

① $V_{CC} = 16V$

$R_B = 470\,K\Omega$

$R_C = 2.7\,K\Omega$

$\beta = 90$

Determine I_{BQ}, I_{CQ}, V_{CEQ}, V_C, V_B and V_E

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{16 - V_{BE}}{470 \times 10^3} = \frac{16 - 0.7}{470 \times 10^3}$$

$V_{BE} = V_B - V_E$

$32\,\mu A$

$\beta I_B = I_C$

$$I_C = 90\left(\frac{16 - V_{BE}}{470 \times 10^3}\right) \Rightarrow 2880\,\mu A \text{ or } 2.8\,mA$$

$$V_{CE} = 16 - 90\left(\frac{16 - V_{BE}}{470 \times 10^3}\right)(2.7 \times 10^3)$$

$$V_{CE} = 16 - \frac{90(16 - V_{BE})}{470} \times 2.7 = 16 - 2.8 \times 2.7 = 16 - 7.56$$

~~$V_C - V_E = 1000$~~ $V_{CE} = 18.44V$

$V_{BE} = V_B - V_E$

as V_E is grounded so $V_E = 0$

$V_B = V_{BE}$

$V_{CE} = V_C - V_E$

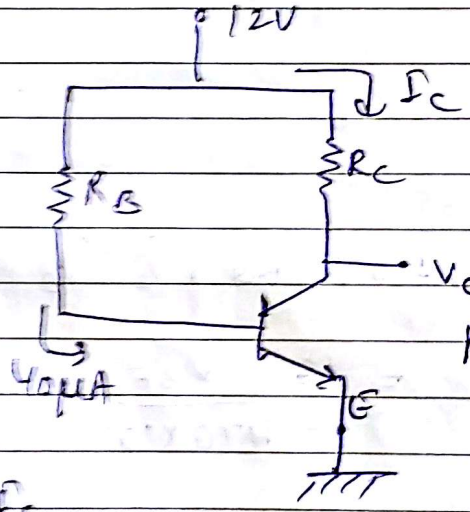
$V_{CE} = V_C$

$V_{BC} = V_B - V_C$

$= V_{BE} - V_{CE}$

$= 0.7 - 8.4$

②



Find I_C
R_C
R_B
V_{CE}

① $I_C = 40 \times 80\ \mu A$

$= 1.2\ mA$

② $R_C = \frac{12V - 6}{I_C}$

$= \frac{6}{1.2\ mA}$

$= \frac{60000}{12}$

$= 5000$

$= 5k\Omega$

③ $R_B = \frac{V_{CE} - V_{BE}}{I_B}$

$= \frac{6 - 0.7}{40\ \mu A}$

$= \frac{5.3\ V}{40\ \mu A}$

$= 0.132 \times 10^6\ \Omega$

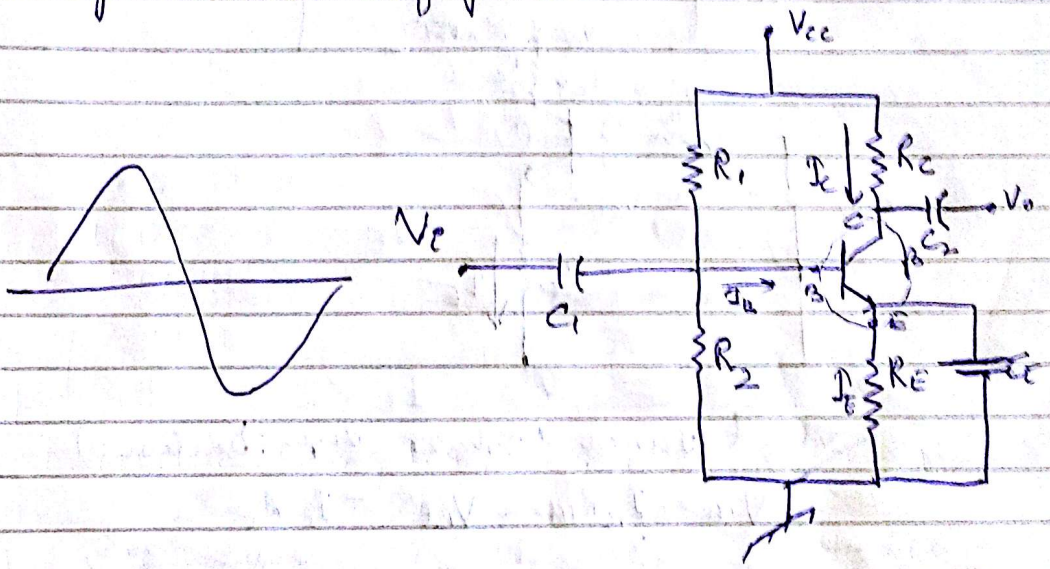
$= 132\ k\Omega$

④ $V_{CE} = V_C - V_E$

$= V_C - 0$

$= 6\ V$

⑤ Voltage Divider configuration



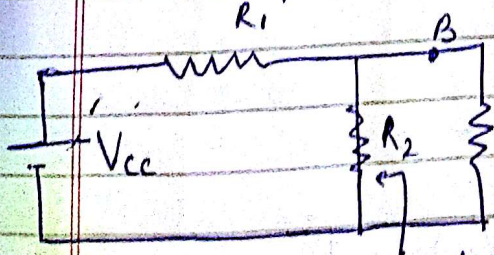
C & C_2 are blocking capacitors ⇒ open circuited for DC Analysis

C_E → bypass capacitor

DC Analysis

Exact Analysis

Consider input section



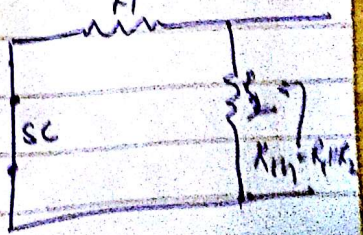
Thevenin

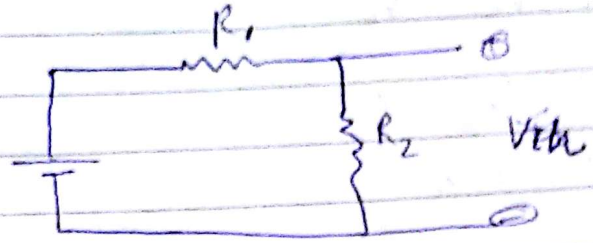
The basic circuit

To calculate R_{th} sc input source

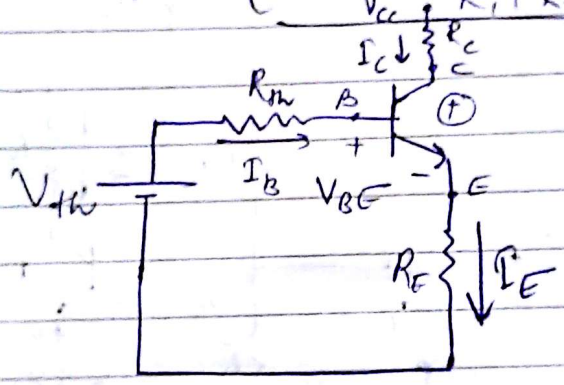
~~Applied~~ Approximate Analysis

[used when $\beta R_E > 10 R_2$]





$$V_{th} = \frac{V_{cc} R_2}{R_1 + R_2}$$



KVL (Inner loop or Input section)

$$V_{th} - I_B R_{th} - V_{BE} - I_E R_E = 0$$

$$I_E = (\beta + 1) I_B$$

$$V_{th} - I_B R_{th} - V_{BE} - (\beta+1) I_B R_E = 0$$

$$I_B = \frac{V_{th} - V_{BE}}{R_{th} + (\beta+1) R_E}$$

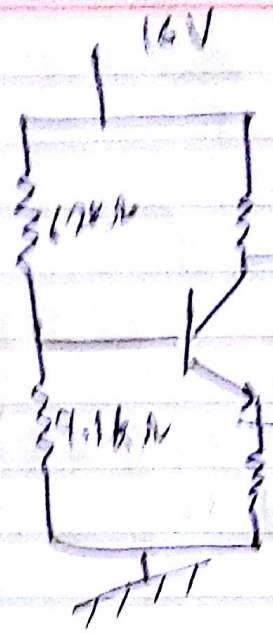
$$I_c = \beta I_B$$

Applying KVL to output section

$$V_{cc} - I_c R_c - V_{CE} - I_E R_E = 0$$

$I_c \approx I_E$

$$V_{CE} = V_{cc} - I_c (R_c + R_E) = 0$$



Determine
(a) I_{BQ}
(b) I_{CQ}
(c) V_{CEQ}
(d) V_C
(e) V_E
(f) V_B

$\beta R_E = (9.1k\Omega)$
$80 \times 0.08 = 91$
$640 \times 10 = 91$

$$\frac{1}{R_{Th}} = \frac{1}{62} + \frac{1}{9.1} = \frac{9.1+62}{69 \times 9.1} = \frac{71.1}{627.9}$$

$$R_{Th} = \frac{627.9}{71.1}$$

$$\boxed{R_{Th} = 8.831k\Omega}$$

$$V_{Th} = \frac{V_{CC} R_2}{R_1 + R_2}$$

$$= \frac{16 \times 9.1}{9.1 + 62}$$

$$\boxed{V_{Th} = 2.04V}$$

$$I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (\beta+1) R_E}$$

$$= 2.04 - 0.7 \qquad 1.34$$

$I_C = \beta I_B$

$= 80 \times 20\,\mu A$

$= 1620\,\mu A$

$= 1.6\,mA$

$V_{CE} = 16 - 1.6(3.9 + 0.68)$

$= 16 - 1.6 \times 4.58$

$= 16 - 7.328$

$= 8.672\,V$

~~$V_{CE} = V_C - V_E$~~

~~8.672~~

$V_E = I_E R_E$

$I_E = I_B + I_C$

$1.621\,mA$

$V_E = 1.621 \times 0.068\,V$

$= 1.101\,V$

$V_C = 0.67 + 0.110$

$= 0.780\,V$

$V_{BE} = V_B - V_E$

$0.7 + 1.10$

$= 1.8\,V$

(2) Approximate Analysis

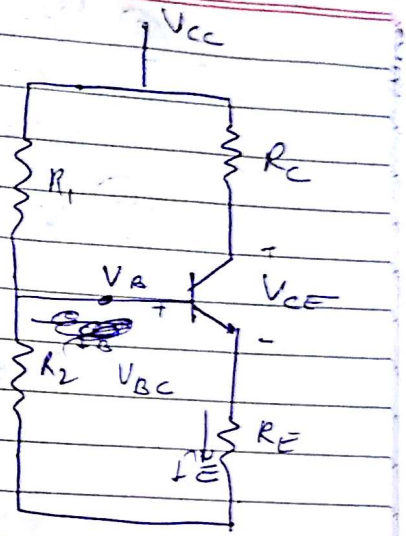
$$V_{BB} = \frac{V_{CC} R_2}{R_1 + R_2}$$

$$V_B - V_{BE} - I_E R_E = 0$$

$$\boxed{I_E = \frac{V_B - V_{BE}}{R_E}}$$

$$\boxed{I_B = \frac{I_E}{\beta + 1}}$$

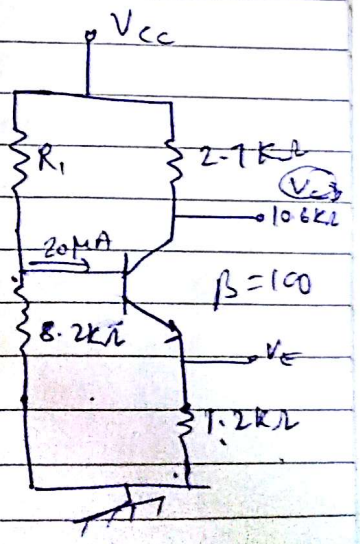
$$\boxed{I_C = \beta I_B}$$



(2) find I_C, I_E, V_E, V_{CC}, V_{CE}, V_B & R_1

$100 \times 1.2 \geq 82$

$120 \geq 82$ →



$V_{CC} = V_C - V_E$

$V_{CC} = 10.6 - V_E$

$10.6 - (V_E = I_E R_E) - 0.7$

$2.02 \times 1.2 = V_B - 0.7$

$\Rightarrow 1.724$

(1) $I_C = 100 \times 20\mu A$

$\boxed{I_C = 2\ mA}$

$\therefore (20\mu A)(101) = \boxed{I_E = 2.02\ mA}$

(2) $V_E = I_E R_E$

$= 2.02 \times 1.2$

$= 1.04$

2.02

④ $V_{CC} - I_C R_C - V_C$

$V_{CC} = 10.6 + 2 \times 2.7$

$V_{CC} = 16V$

⑤ $V_{CE} = V_C - V_E$ $= 10.6 - 2.4$

$= 8.2V$

⑤ $V_{BE} = V_B - V_E$

$V_B = V_{BE} + V_E$

$= 3.2V$

⑥ $V_{BB} = \frac{16 \times 8.2}{8.2 + R_1}$

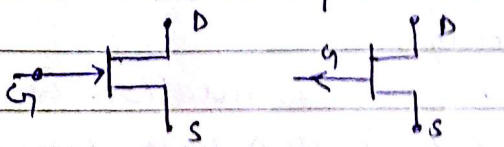
$3.2 = \frac{16 \times 8.2}{8.2 + R_1}$ $= \frac{131.2}{8.2 + R_1}$

$26.24 + 3.2R_1 = 131.2$

$R_1 = 32.8\Omega$

FET (Field Effect Transistor)

- JFET (Junction FET)
  - R_i (10^6 to 10^8 Ω)
  - n-channel
  - p-channel



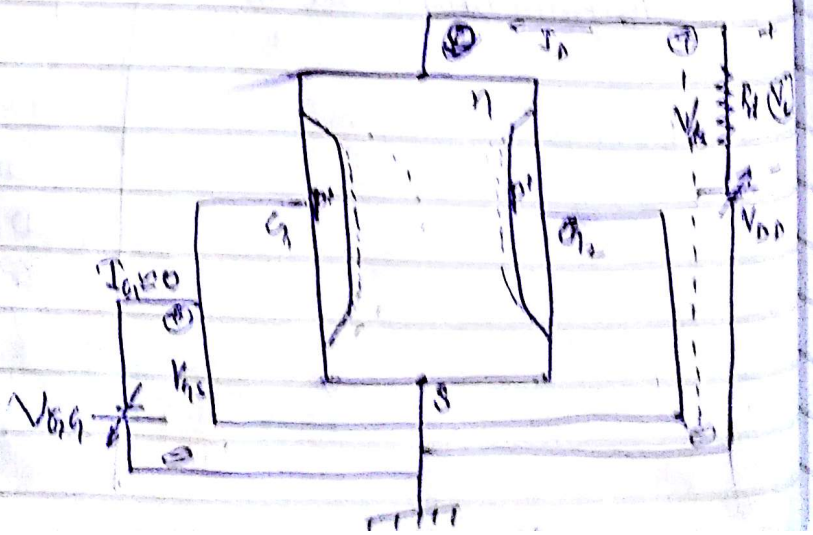
- MOSFET (Metal oxide semiconductor FET)
  - $R_i \rightarrow 10^{10}$ to 10^{15} Ω
  - Depletion MOSFET
    - n-channel
    - p-channel
  - Enhancement MOSFET
    - n-channel
    - p-channel

BJT	FET
1. Bipolar Devices	Unipolar Devices
2. presence of leakage current.	Absence of leakage current
3. Thermal stability is less	comparatively more thermally stable
4. Current – controlled devices	voltage - controlled devices
5. Asymmetrical Device	Symmetrical Devices
E, B, C	S, D, G ~~Emit~~ Source Drain Gate

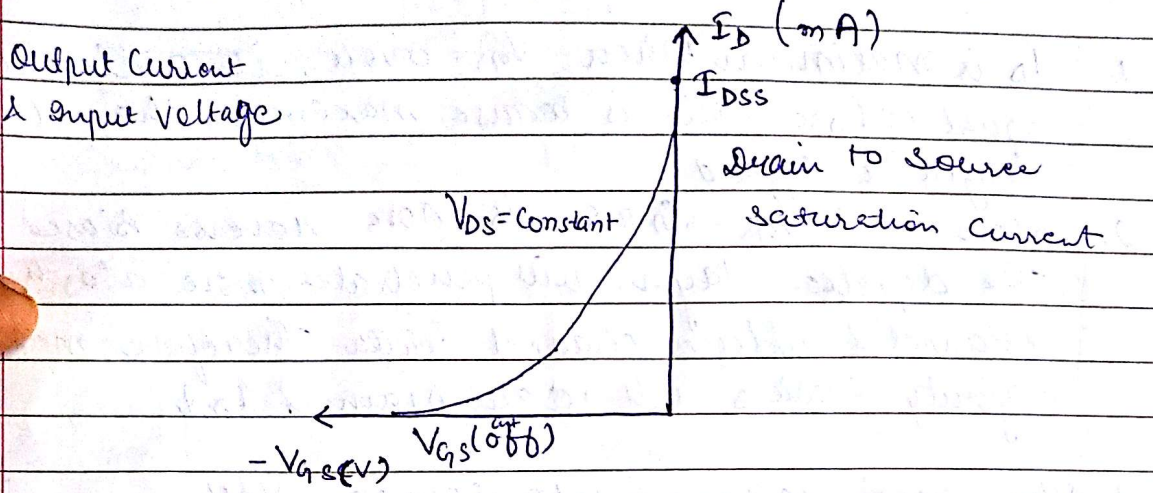
1. FET is a voltage controlled device as operation of FET depends on electric field intensity produced in the channel.
2. FET is a unipolar device hence it is a majority carrier device i.e. there is no leakage current due to minority charge carriers.
3. Due to absence of leakage current FET has excellent thermal stability.
4. When compare to BJT, FET is smaller in size easier to fabricate and it is a better device as an amplifier.
5. It is three terminals
   1. Source(S) - It is source of majority carriers
   2. Drain(D) - It is the terminal which drains of majority carriers
   3. Gate(G) - It is the terminate which controls the majority carriers moving from source to drain or indirectly controls the drain current.

Channel - It is the region in b/w two gates.

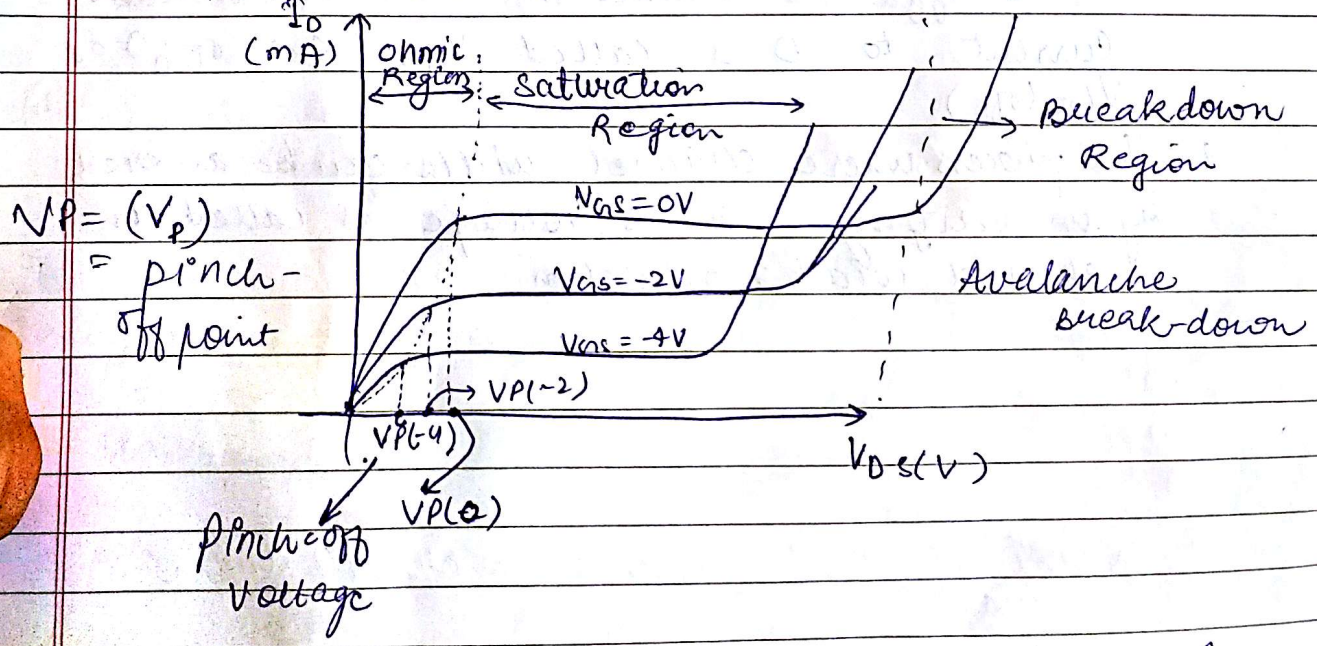
n-channel JFET :-



Transfer characteristics :-



Output characteristics :-



- In open circuit JFET channel cross sectional Area is maximum. When V_{DS} is applied channel width decreases. Depletion layer will penetrate more into the channel near the Drain
- Of JFET channel is wedge-shaped
- In JFET gate to source voltage is always operated under Reverse Bias
- The magnitude of gate leakage current I_G is in (nA) (neglected)

Explanation of Transfer chara

1. I_D is maximum when V_{GS} = 0 volt, its value is equal to I_{DSS} this is because maximum channel length is offered
2. when we ↑ V_{GS} → G to S is more reverse biased The depletion layer will penetrate more into the channel & reduces channel width Therefore more majority carriers will reach Drain & I_D ↓.
3. The min ~~voltage~~ Gate to source Voltage required to cut-off the channel or to reduce the drain current to 0 is called V_{GS} (cut-off) or V_{GS} (off)
4. The process where channel width can be altered by ~~to~~ varying G to S Voltage is called as channel width modulation